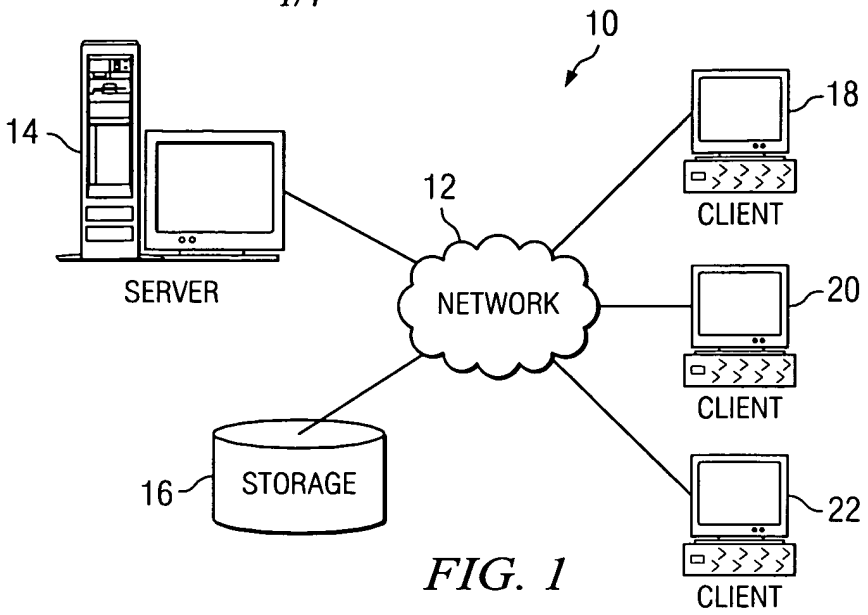
10
14
SERVER
12
NETWORK
18
CLIENT
20
CLIENT
22
CLIENT
16
STORAGE

FIG. 1

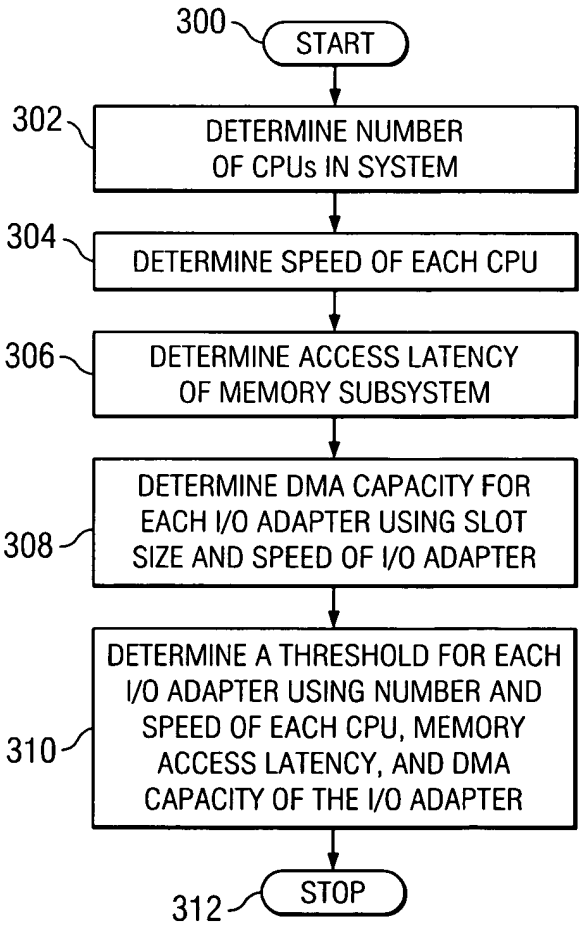
300
START
302
DETERMINE NUMBER OF CPUs IN SYSTEM
304
DETERMINE SPEED OF EACH CPU
306
DETERMINE ACCESS LATENCY OF MEMORY SUBSYSTEM
308
DETERMINE DMA CAPACITY FOR EACH I/O ADAPTER USING SLOT SIZE AND SPEED OF I/O ADAPTER
310
DETERMINE A THRESHOLD FOR EACH I/O ADAPTER USING NUMBER AND SPEED OF EACH CPU, MEMORY ACCESS LATENCY, AND DMA CAPACITY OF THE I/O ADAPTER
312
STOP

FIG. 3

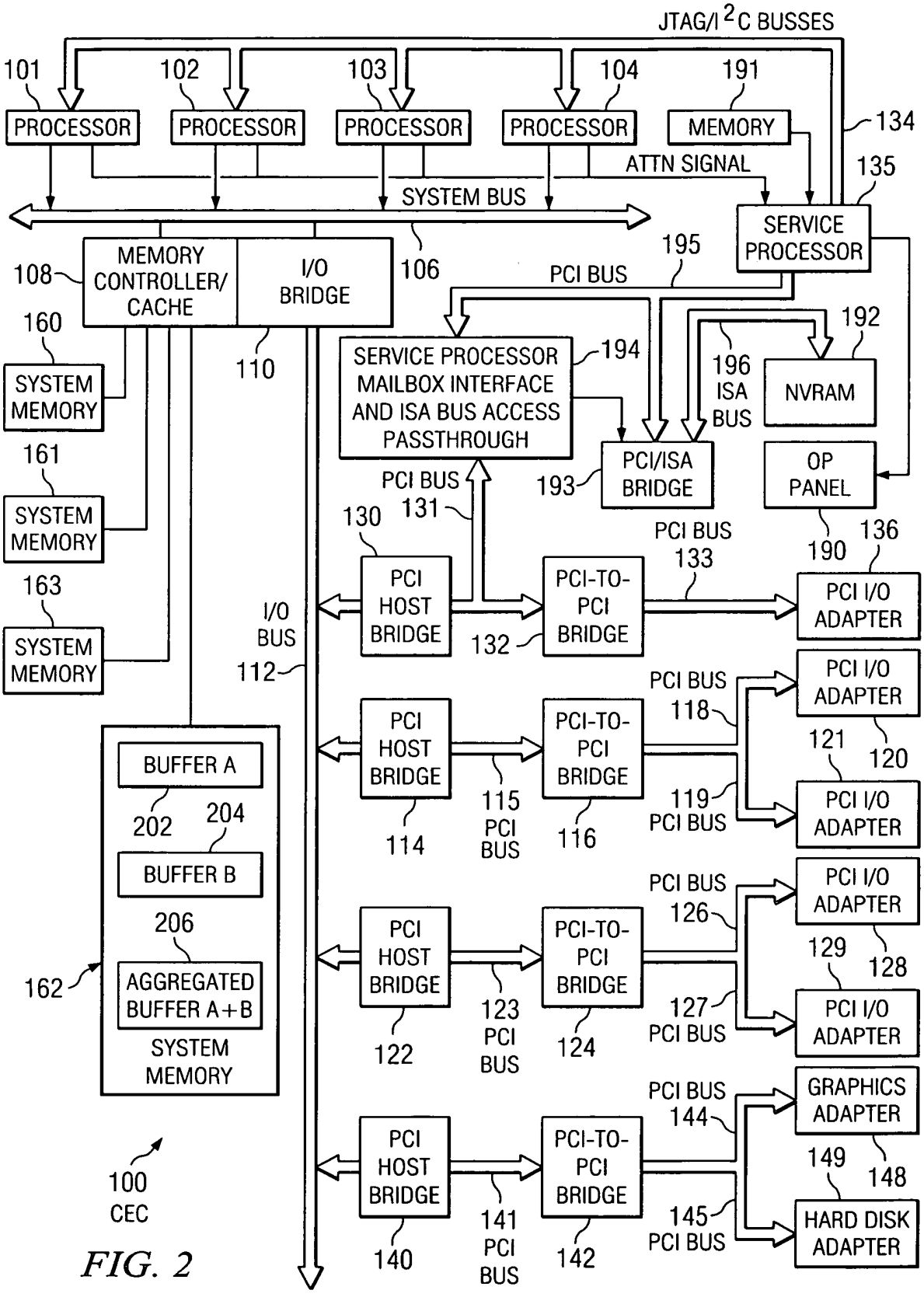
JTAG/I 2C BUSSES
101
102
103
104
191
PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
MEMORY
134
ATTN SIGNAL
135
SYSTEM BUS
106
SERVICE PROCESSOR
195
PCI BUS
108
MEMORY CONTROLLER/ CACHE
I/O BRIDGE
110
160
SYSTEM MEMORY
161
SYSTEM MEMORY
163
SYSTEM MEMORY
SERVICE PROCESSOR MAILBOX INTERFACE AND ISA BUS ACCESS PASSTHROUGH
194
196
ISA BUS
192
NVRAM
PCI/ISA BRIDGE
193
OP PANEL
190
136
PCI BUS
133
PCI BUS
131
130
PCI HOST BRIDGE
PCI-TO-PCI BRIDGE
132
PCI I/O ADAPTER
I/O BUS
112
PCI BUS
118
PCI I/O ADAPTER
121
120
PCI HOST BRIDGE
PCI-TO-PCI BRIDGE
115
PCI BUS
114
116
119
PCI BUS
PCI I/O ADAPTER
BUFFER A
202
204
BUFFER B
206
162
AGGREGATED BUFFER A+B
SYSTEM MEMORY
PCI BUS
126
PCI I/O ADAPTER
129
128
PCI HOST BRIDGE
PCI-TO-PCI BRIDGE
123
PCI BUS
122
124
127
PCI BUS
PCI I/O ADAPTER
PCI BUS
144
GRAPHICS ADAPTER
149
148
PCI HOST BRIDGE
PCI-TO-PCI BRIDGE
141
PCI BUS
140
142
145
PCI BUS
HARD DISK ADAPTER
100
CEC

FIG. 2

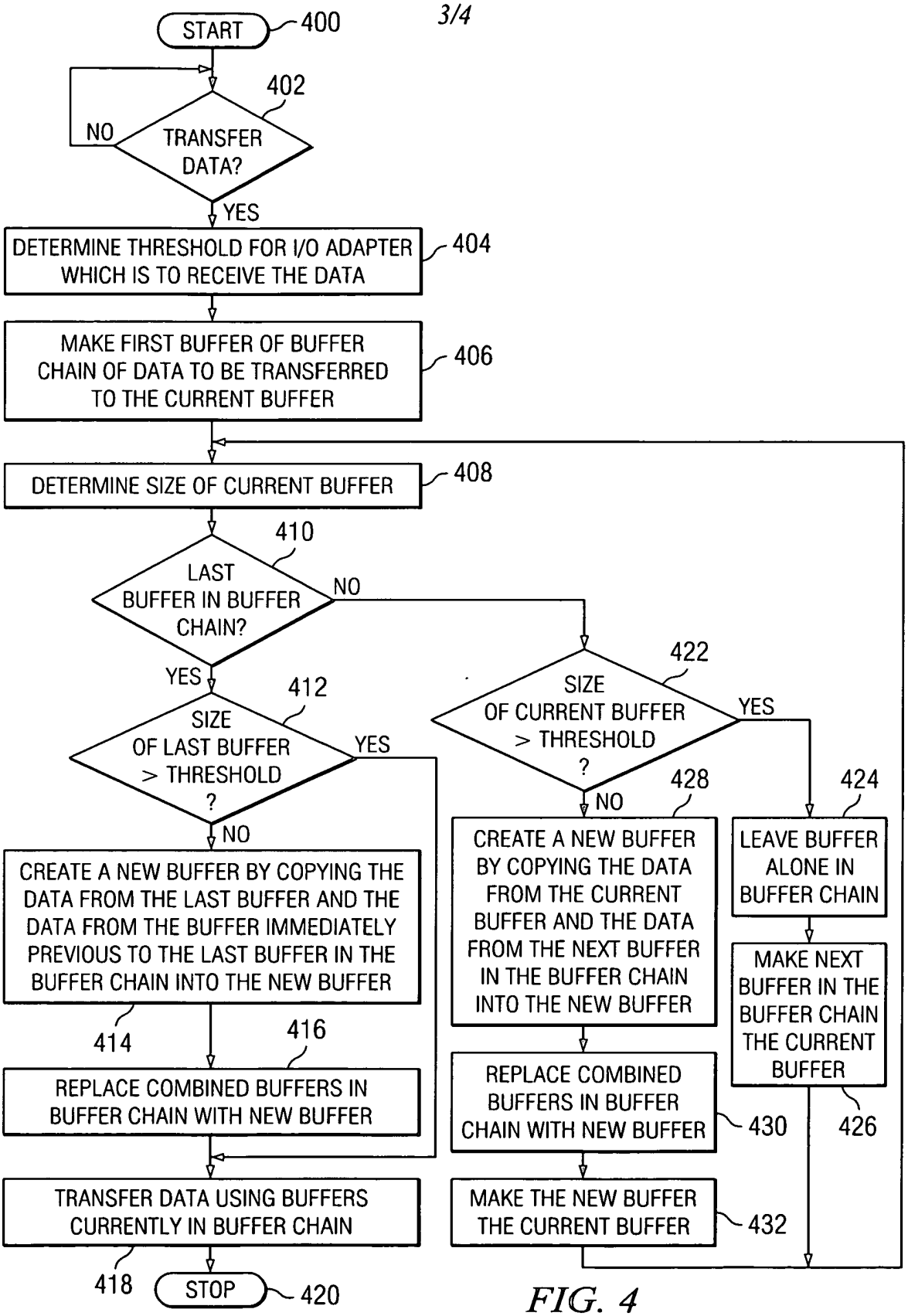
START
400
402
TRANSFER DATA?
NO
YES
DETERMINE THRESHOLD FOR I/O ADAPTER WHICH IS TO RECEIVE THE DATA
404
MAKE FIRST BUFFER OF BUFFER CHAIN OF DATA TO BE TRANSFERRED TO THE CURRENT BUFFER
406
DETERMINE SIZE OF CURRENT BUFFER
408
410
LAST BUFFER IN BUFFER CHAIN?
NO
YES
412
SIZE OF LAST BUFFER > THRESHOLD ?
YES
NO
CREATE A NEW BUFFER BY COPYING THE DATA FROM THE LAST BUFFER AND THE DATA FROM THE BUFFER IMMEDIATELY PREVIOUS TO THE LAST BUFFER IN THE BUFFER CHAIN INTO THE NEW BUFFER
414
416
REPLACE COMBINED BUFFERS IN BUFFER CHAIN WITH NEW BUFFER
TRANSFER DATA USING BUFFERS CURRENTLY IN BUFFER CHAIN
418
STOP
420
422
SIZE OF CURRENT BUFFER > THRESHOLD ?
YES
NO
428
CREATE A NEW BUFFER BY COPYING THE DATA FROM THE CURRENT BUFFER AND THE DATA FROM THE NEXT BUFFER IN THE BUFFER CHAIN INTO THE NEW BUFFER
REPLACE COMBINED BUFFERS IN BUFFER CHAIN WITH NEW BUFFER
430
MAKE THE NEW BUFFER THE CURRENT BUFFER
432
424
LEAVE BUFFER ALONE IN BUFFER CHAIN
MAKE NEXT BUFFER IN THE BUFFER CHAIN THE CURRENT BUFFER
426

FIG. 4

CPU		MEMORY ACCESS LATENCY	DMA CAPABILITY		AGGREGATION THRESHOLD
NUMBER	SPEED		WIDTH	SPEED	
4	1.45 MHz	5 MICROSECONDS	32 BITS	33 MHz	2049 BYTES
				66 MHz	1792 BYTES
				133 MHz	1408 BYTES
			64 BITS	33 MHz	1792 BYTES
				66 MHz	1408 BYTES
				133MHz	1025 BYTES

FIG. 5

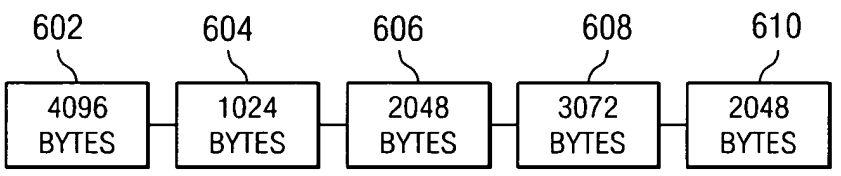

FIG. 6a

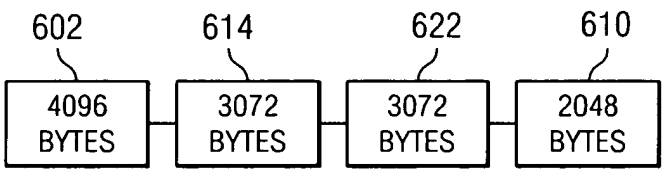

FIG. 6b

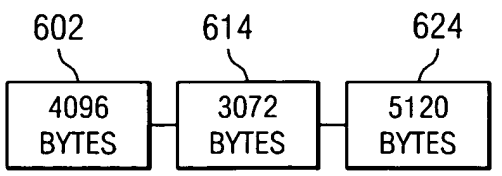

FIG. 6c